UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,468	02/04/2004	Hiroyuki Tomimatsu	118459	1357

25944 7590 01/19/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
LEE, KYOUNG	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/770,468	TOMIMATSU, HIROYUKI
	Examiner	Art Unit
	Kyoung Lee	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *8-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/3/05, 2/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-7 in the reply filed on December 07, 2005 is acknowledged. The traversal is on the ground(s) that the inventions are so closely related to each other that they would not be a serious burden for the Examiner to examine all of the claims at one time. This is not found persuasive.

A restriction requirement between distinct sets of process claims was issued in the office action mailed September 24, 2005. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct invention,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." *See Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner notes that the claim 1-7 and 8-10 require a different field of search. For instance search for claims 1-7 is in 438/106 and 8-14 in 257/678.

Further, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prime facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803.

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 rejected under 35 U.S.C. 102(e) as being anticipated by Kurita et al. (U.S. Patent Appl. 2003/0189259).

In re claim 1, Kurita disclose a method of manufacturing a semiconductor device, comprising: providing liquid resin (9) on a first semiconductor chip (7) having a plurality of pads (12), which is mounted on a substrate having wiring pattern (2);

Mounting a second semiconductor chip (11) over the first semiconductor chip through the liquid resin, in an overlapping manner and separated from the pads; and hardening the liquid resin (9) to form a spacer between the first semiconductor chip and the second semiconductor chip, and to fix the first and second semiconductor chips together (see figure 2A-2G, and paragraph [0098] - [0103]).

In re claim 2, Kurita disclose the method of forming the spacer such that the first semiconductor chip is oriented generally in parallel with the second semiconductor (see figure 2A-2G, and paragraph [0096] lines 1-10).

In re claim 3, Kurita disclose the method of forming liquid resin including a plurality of balls (8), such that the balls are present between the first and second semiconductor chips (see figure 2C, and paragraph [0100]).

In re claim 4, Kurita disclose the method of forming the balls being elastic (see paragraph [0094]).

In re claim 5, Kurita disclose the method of electrically connecting the pads on the first semiconductor chip and the wiring patterns with wires (13), before the mounting of the second semiconductor chip (see figure 2A-2E, and paragraph [0098] - [0102]).

In claim 6, Kurita disclose the method of forming a dielectric layer (23) on a surface of the second semiconductor chip that face the first semiconductor chip (see figure 7 and [0117]-[0119]).

In claim 7, Kurita disclose the method of forming a sealing section (16) on the substrate to seal the first and second semiconductor chips (see figure 2G and [0104]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (U.S. Patent Appl. 2002/0125556) in view of Glenn et al. (U.S. Patent 6,472,758).

In re claim 1, Oh disclose a method of manufacturing a semiconductor device, comprising: providing liquid resin (3) on a first semiconductor chip having a plurality of pads (1), which is mounted on a substrate having wiring pattern (7);

Mounting a second semiconductor chip (2) over the first semiconductor chip through the liquid resin, in an overlapping manner and separated from the pads; and hardening the liquid resin (3) to form a spacer between the first semiconductor chip and the second semiconductor chip, and to fix the first and second semiconductor chips together, but does not teach the method of hardening liquid resin after mounting a second semiconductor chip (see figure 1, and [0020]-[0022] and [0064]). Glenn discloses that the adhesive can be used as liquid resin and discloses the method of hardening liquid resin (40) after mounting a second semiconductor chip (see figure 5-6 and column 5 lines 20-27 and column 6 lines 40-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to including a hardening liquid resin after mounting a second semiconductor chip in the method of Oh in order to simultaneously conduct a step of forming a spacer and a step of fixing the first and

second semiconductor chips together and therefore the semiconductor device can be effectively manufactured.

In re claim 2, Oh disclose the method as claimed and rejected above and forming the spacer such that the first semiconductor chip is oriented generally in parallel with the second semiconductor, but does not teach the method of hardening liquid resin after mounting a second semiconductor chip (see figure 1). Glenn discloses method of hardening liquid resin (40) after mounting a second semiconductor chip (see figure 5-6 and column 6 lines 40-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to including a hardening liquid resin after mounting a second semiconductor chip in the method of Oh in order to simultaneously conduct a step of forming a spacer and a step of fixing the first and second semiconductor chips together and therefore the semiconductor device can be effectively manufactured.

In re claim 3, Oh disclose the method as claimed and rejected above, but does not teach the method of the liquid resin including a plurality of balls, such that the balls are present between the first and second semiconductor chip. Glenn discloses the method of the liquid resin including a plurality of balls (48), such that the balls are present between the first (14) and second (16) semiconductor chip (see figure 6 and column 7, lines 7-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to including a plurality of balls in the liquid resin, such that the balls are present between the first and second semiconductor chip in the method of Oh in order to control the space between first and second semiconductor chip.

In re claim 4, Oh disclose the method as claimed and rejected above, but does not teach the method of the ball being elastic. Glenn discloses the method of the ball being elastic (see column 7, lines 26-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to the ball being elastic in the method of Oh in order to reduce or prevent damage on the semiconductor chips.

In re claim 5, Oh disclose the method as claimed and rejected above and electrically connecting the pads on the first semiconductor chip and the wiring patterns with wires (5), before the mounting of the second semiconductor chip, but does not teach the method of hardening liquid resin after mounting a second semiconductor chip (see [0024]-[0025] and [0037]). Glenn discloses method of hardening liquid resin (40) after mounting a second semiconductor chip (see figure 5-6 and column 6 lines 40-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to including a hardening liquid resin after mounting a second semiconductor chip in the method of Oh in order to simultaneously conduct a step of forming a spacer and a step of fixing the first and second semiconductor chips together and therefore the semiconductor device can be effectively manufactured.

In re claim 6, Oh disclose the method as claimed and rejected above and a dielectric layer (4) on a surface of the second semiconductor chip that face the first semiconductor chip, but does not teach the method of hardening liquid resin after mounting a second semiconductor chip (see figure 1 and [0026]-[0027]). Glenn discloses method of hardening liquid resin (40) after mounting a second semiconductor chip (see figure 5-6 and column 6 lines 40-44). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to including a hardening liquid resin after mounting a second semiconductor chip in the method of Oh in order to simultaneously conduct a step of forming a spacer and a step of fixing the first and second semiconductor chips together and therefore the semiconductor device can be effectively manufactured.

In re claim 7, Oh disclose the method as claimed and rejected above and a sealing section (8) on the substrate to seal the first and second semiconductor chips, but does not teach the method of hardening liquid resin after mounting a second semiconductor chip (see figure 5 and [0073]). Glenn discloses method of hardening liquid resin (40) after mounting a second semiconductor chip (see figure 5-6 and column 6 lines 40-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to including a hardening liquid resin after mounting a second semiconductor chip in the method of Oh in order to simultaneously conduct a step of forming a spacer and a step of fixing the first and second semiconductor chips together and therefore the semiconductor device can be effectively manufactured.

Response to Amendment

By the response of first office action mailed on 12/07/2005, the examiner carefully reviewed and withdrawn the first office action filed on 09/07/2005. Argument is moot.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Glenn (U.S. Patent Number 5,867,368).

Glenn disclose that Hysol 4450, Hysol 4451, or Hysol 4323 is a resin material.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyoung Lee whose telephone number is (571) 272-1982. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KL

Jennifer M. Kennedy
JENNIFER KENNEDY
PRIMARY EXAMINER